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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/714,936	11/18/2003	Hidemi Oyama	XA-9965	3706

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MILES & STOCKBRIDGE PC
1751 PINNACLE DRIVE
SUITE 500
MCLEAN, VA 22102-3833

EXAMINER	
HASSAN, AURANGZEB	
ART UNIT	**PAPER NUMBER**
2182	

DATE MAILED: 01/30/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/714,936	OYAMA ET AL.	
	Examiner	Art Unit	
	Aurangzeb Hassan	2182	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 November 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-13* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *11/18/2003*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1 thru 13 are rejected under 35 U.S.C. 102(b) as being anticipated by Coteus et al. (US Patent Number 6,276,844, hereinafter "Coteus").

3. As per claim 1, Coteus teaches a data processor comprising,

a central processing unit (CPU, figure 1, column 4, likes 14 –16); and

a memory card interface controller (memory-processor control unit, column 4, line 19) connectable to a clock synchronized (column 4 ,lines 26 – 28) memory card,

wherein said memory card interface controller transmits a clock signal to said memory card to acquire read data therefrom in synchronism with said clock signal, said memory card interface controller being switchable between a raising edge and a falling edge of said clock signal when acquiring said read data in synchronous relation with said clock signal (column 5, lines 60 – 67, column 6, lines 1 – 4) .

4. As per claim 2, Coteus teaches a data processor wherein said memory card interface controller is switchable between different frequencies of said clock signal (75Mhz and 100Mhz, column 8, lines 35 – 41).

5. As per claim 3, Coteus teaches a data processor wherein said central processing unit switches between the raising edge and the falling edge of the clock signal in response to a data read error during read data acquisition in synchronism with the clock signal (column 4, lines 26 – 56).

6. As per claim 4, Coteus teaches a data processor wherein said central processing unit switches from a high frequency to a low frequency of the clock signal in response to a data read error (75Mhz, column 7, lines 41 – 46).

7. As per claim 5, Coteus teaches a data processor wherein said central processing unit switches between the raising edge and the falling edge of the clock signal (figures 8 – 11) in response to a data read error during read data acquisition in synchronism with said clock signal, the central processing unit further switching from a high frequency to a low frequency of the clock signal in response to a data read error following the switching between the raising edge and the falling edge of the clock signal (column 8, lines 18 – 41).

8. As per claim 6, Coteus teaches a data processor wherein said central processing unit switches from a high frequency to a low frequency of the clock signal (figures 8 – 11) in response to a data read error, said central processing unit further switching between the raising edge and the falling edge of the clock signal in response to a data

read error after the frequency switching during read data acquisition in synchronism with the clock signal (column 8, lines 18 – 41).

9. As per claim 7, Coteus teaches a data processor comprising:

a first register accessible by said central processing unit, the first register being loaded with control data for determining whether said read data is to be acquired in synchronism with the raising edge or with the falling edge of said clock signal (buffers, column 8, lines 18 – 28).

10. As per claim 8, Coteus teaches a data processor comprising:

first and second registers accessible by said central processing unit, said first register being loaded with control data for determining whether said read data is to be acquired in synchronism with the raising edge or with the falling edge of said clock signal, said second register being loaded with control data for determining whether said clock signal is to have a high frequency or a low frequency (arrangement according to figure 14, column 8, lines 20 – 42).

11. As per claim 9, Coteus teaches a data processor comprising:

a nonvolatile memory which is electrically rewritable and which serves as a storage area for accommodating a control program executed by said central processing unit in order to generate said control data (column 4, lines 14 – 26).

12. As per claim 10, Coteus teaches a data processor wherein said memory card interface controller transmits data to said memory card in synchronism with the clock signal, said memory card interface controller being switchable between the raising edge and the falling edge of said cock signal when transmitting the data in synchronous relation with said clock signal (column 4, lines 26 – 31, column 8, lines 18 – 41).

13. As per claim 11, Coteus teaches a memory card for receiving a clock signal from a memory card host device and transmitting read data to said memory card host device,

wherein said memory card determines whether to synchronize with a raising edge or with a falling edge of said clock signal when transmitting said read data (column 8, lines 18 – 41).

14. As per claim 12, Coteus teaches a memory card wherein said memory card host device instructs said memory card to determine whether to synchronize with the raising edge or with the falling edge of said clock signal (column 4, lines 26 – 31).

15. As per claim 13, Coteus teaches a memory card wherein said memory card acquires data from the memory card host device in synchronism with said clock signal, said memory card further determining whether to synchronize with the raising edge or with the falling edge of said clock signal when acquiring said data (column 4 lines 14 – 56).

Conclusion

16. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Aurangzeb Hassan whose telephone number is (571)272-8625. The examiner can normally be reached on Monday - Friday 9 AM to 5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kim Huynh can be reached on (571)272-4147. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

1/20/2006
AH

TAMMARA PEYTON
PRIMARY EXAMINER